REMARKS

Claims 1-20 are pending in the instant application. Claims 1-20 are rejected. Claims 2-6, 8-13, 15 and 19 are amended. No new matter has been added as a result of these amendments.

Specification

The specification is objected to in the outstanding Office Action as containing informalities. The specification has been amended to obviate the cited objection (see attached amendment). Consequently, the Applicant requests the withdrawal of the outstanding objection to the specification.

Drawings

The drawings are objected to in the outstanding Office Action as not showing the recited series of flip flops specified in the claims. However, the series of flip flops such as are recited in the Claims are shown at Figure 1, structures 124 and 128. Accordingly, as the drawings indeed do show every feature of the invention specified in the Claims, the Applicant respectfully requests that the objection to the drawings be withdrawn.

103 Rejection

Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Korhonen et al. (U.S. Patent 5,378,935). The Applicant has reviewed the cited reference and respectfully submits that the embodiments of the present invention as are set forth in Claims 1-20 are neither anticipated nor rendered obvious by Korhonen et al.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention that includes:

> ... logic means, receiving the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto, the logic means for producing a signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock, phase shifted current clock, the new clock and the phase shifted new clock have the same state.

Claims 2-6 depend from Claim 1, Claims 8-13 depend from Claim 7, Claim 15 depends from Claim 14, and Claims 17-20 depend from Claim 16 and set forth additional limitations of the claimed invention.

Korhonen et al. does not anticipate or render obvious a circuit that allows a processor that forms a part of a microcontroller to change its operating frequency and includes "logic means, receiving the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto, the logic means for producing a signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock, phase shifted current clock, the new clock and the phase shifted new clock have the same state" as is recited in Claim 1 (Claims 7, 14 and 16 contain similar limitations). In order to meet the limitations of Claim 1 Korhonen et al. must show or suggest, either inherently or expressly, in addition to the other limitations of Claim 1: (1) a logic means that receives current clock, new clock, phase shifted new clock and processor signals, and that (2) the logic means produces a signal that latches the new speed into the current speed latch when the signals in (1) have the same state.

Korhonen et al. only shows a system that facilitates clock frequency adjustment of the various clocks supplied to sub-circuits of an electrical circuit system. Specifically, Korhonen et al. is concerned with the selection of the appropriate clock frequency to supply to each of a plurality of sub-circuits of an electrical circuit system. This stands in contrast to the system that is claimed by the Applicant that involves a processor's adjustment of its own operating frequency based on the attainment of specifically defined conditions (when certain clocks specifically defined in the claims "have the same state") that are clearly set forth in Claim 1 (Claims 7, 14 and 16 contain similar limitations).

In fact, nowhere in the Korhonen et al. reference is a circuit that includes logic means that receives a current clock, a phase shifted current clock, a new clock, a phase shifted new clock and a signal (from a processor directing a speed change) as inputs to the logic means for producing a signal that latches a new speed into the current speed latch at a point in time after (the occurrence of) a speed change signal when the current clock, the phase shifted current clock, the new clock and the phase shifted new clock have the same state shown or suggested as is recited in Claim 1 (Claims 7, 14 and 16 contain similar limitations). Consequently, Korhonen et al. does not anticipate or render obvious the embodiments of the Applicant's invention as are set forth in Claims 1, 7, 14 and 16.

The modification of Korhonen et al. reference as proposed in the Office Action does not overcome the deficiencies of the Korhonen et al. reference outlined above. It is contended in the Office Action (see page 4) that: (1) if first and second phase shifters were to be added to the system disclosed in Korhonen et al. the system's operation would not be impacted, and that (2) phase shifters are known as a means of delaying clock signals (it is noted that these contentions

appear to be contradictory). It is important to note that it is not explained how the proposed modification would cure the deficiencies of the Korhonen et al. reference outlined above.

The Applicant respectfully disagrees with the assertion that the imposition of phase shifters into the design of Korhonen et al. would not impact the systems operation since the imposition of phase shifters would have timing consequences and almost no matter how connected would introduce signal changes that are likely to disturb the operation of a system that already has a design balance (e.g., placement and connection of components and timing and action of signals). Moreover, nowhere in the Korhonen et al. reference is there any teaching or suggestion that additional clock delay need be added to any of the signals disclosed therein (or how that would be accomplished using phase shifters). As such, the Applicant respectfully submits that interposing such foreign components that would have timing consequences (the phase shifters) into the circuit design of Korhonen et al. as suggested in the Office Action would not be obvious to one of ordinary skill in the art. More importantly, the Applicant respectfully submits that even if the modifications were made it would not cure the deficiencies of Korhonen et al. outlined above. Consequently, Korhonen et al. modified as suggested in the Office Action does not anticipate or render obvious the embodiments of the Applicant's invention as are set forth in Claims 1, 7, 14 and 16.

Accordingly, the Applicant also respectfully submits that Korhonen et al. does not anticipate or render obvious the present claimed invention as is recited in Claims 2-6, 8-13, 15 and 17-20 dependent on Claims 1, 7, 14 and 16 respectively and that these Claims overcome the rejection under 35 U.S.C. 103(a) as being dependent on allowable base claims.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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